CLEAN COPY OF ALL PENDING CLAIMS

28. A method of fabricating a CMOS inverter, the method comprising the steps of:

providing a heterostructure including a Si substrate, a $Si_{1-x}Ge_x$ layer on the Si substrate, and a strained layer on the $Si_{1-x}Ge_x$ layer, the heterostructure comprising an interface, located between the strained layer and the Si substrate, that exhibits a roughness less than 1 nm, whereby the strained layer exhibits a surface roughness less than 1 nm; and

integrating a pMOSFET and an nMOSFET in the heterostructure, wherein a channel of the pMOSFET and a channel of the nMOSFET are formed in the strained surface layer.

29. The method of claim 28 wherein the $Si_{1-x}Ge_x$ layer is relaxed.

30. The method of claim 28 wherein the heterostructure further comprises an underlying insulator layer.

31. The method of claim 28 wherein $0.1 < x < 0.5$.

32. A method of fabricating an integrated circuit comprising:

providing a heterostructure having a Si substrate and a strained layer thereover, the strained layer exhibiting a surface roughness less than 1 nm; and

forming a p transistor and an n transistor in the heterostructure, wherein the strained layer comprises a channel of at least one of the transistors, the transistors being interconnected in a CMOS circuit.

33. The method of claim 32 wherein the heterostructure further comprises an insulating layer below the strained layer.

34. The method of claim 42 wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

35. The method of claim 32 wherein the strained layer comprises Si.

36. The method of claim 32 wherein $0.1 < x < 0.5$.

37. The method of claim 32 wherein the CMOS circuit comprises a logic gate.

38. The method of claim 37 wherein the logic gate is a NOR gate.

39. The method of claim 37 wherein the logic gate is an XOR gate.

40. The method of claim 37 wherein the logic gate is a NAND gate.

41. The method of claim 32 wherein the p-channel transistor serves as a pull-up transistor in the CMOS circuit and the n-channel transistor serves as a pull-down transistor in the CMOS circuit.

42. The method of claim 32 wherein the heterostructure further comprises a $Si_{1-x}Ge_x$ layer below the strained layer.

43. The method of claim 32 wherein an interface including an unexposed face of the strained layer exhibits a roughness less than 1 nm.